AMENDMENTS TO THE CLAIMS:

This listing of the claims replaces all prior versions, and listings, of claims in the application.

1. (currently amended) ~~An~~ A system ~~interface between a master and one or more slave modules~~ comprising:

~~a master;~~

~~a slave having a set of addressable registers including egress mailbox registers, ingress mailbox registers, and indirect access address registers;~~

~~a direct memory access (DMA) engine coupled to a the master by a first bus and to the slaveby a second bus, with the second bus comprising:~~

a Packet Voice Data Module (PVDM) having a set of bi-directional data ~~lines~~ inputs/outputs configured as an interface between a master device coupled to a DMA engine and a slave device having a set of addressable registers including egress mailbox registers, ingress mailbox registers, and indirect access address registers, with the interface comprising ~~for transmitting data between the slave and the DMA engine~~;

a set of master address ~~lines~~ inputs configured to couple the PVDM to the DMA engine, with the master address for-transmitting address data from the DMA engine to the slave;

a master data strobe input configured to couple the PVDM to the DMA engine, with the master data strobe for strobing data;

a master read/write signal input configured to couple the PVDM to the DMA engine, with master read/write signal for indicating whether data is to be read from or written to the slave;

a set of slave select signal inputs configured to couple the PVDM to the DMA engine, with slave select signals for selecting one of a plurality of slaves ~~connected to the second bus~~;

a slave wait signal output configured to couple the PVDM to the DMA engine, with the slave wait signal asserted by a slave to delay a data transfer;

a slave reset signal input configured to couple the PVDM to the DMA engine, with the slave reset signal resetting the slave when asserted;

a clock ~~output~~ signal line output configured to couple the PVDM to the DMA engine and to receive a clock signal; [,]and

a clock ~~input~~ signal line input configured to couple the PVDM to the DMA engine and to receive a clock input signal[;]

~~where the DMA engine performs direct data transfers to the slave by asserting a slave select signal to the slave and transferring data over the set of bi-directional data lines to the slave egress or ingress data registers and performs indirect data transfers to slave memory by writing address data over the set of bi-directional data lines to the indirect address register of the slave and where the slave utilizes its own memory map and the address data to transfer data between a location indicated by the address data and the DMA engine~~.

2. (currently amended) The system ~~interface~~ of claim 1 further comprising a ~~where the~~ DMA engine configured to perform direct data transfers to the slave by asserting a slave select signal to the slave and to transfer data to the slave egress or ingress data registers and to perform indirect data transfers to slave memory by writing address data to the indirect address register of the slave and to negotiate ~~negotiates~~ with a slave to implement either an asynchronous, synchronous, or source synchronous data transfer.

3. (currently amended) The system ~~interface~~ of claim 2 ~~claim 1~~ with ~~where~~ the DMA engine configured to negotiate ~~negotiates~~ with all slaves during reset to determine a ~~the~~ maximum bus width available to transfer data.

4. (currently amended) The system ~~interface~~ of claim 1 further comprising ~~where~~:

~~the~~ a slave including a ~~includes~~ status register and a message signal interrupt (MSI) register; and

where the slave is configured to utilize its own memory map and the address data to transfer data between a location indicated by the address data and the DMA engine and to assert ~~asserts~~ a bit in the status register to indicate it is ready for a transaction and where the DMA engine is configured to assert ~~asserts~~ a bit in the MSI register to indicate when a transaction is complete.

5. (currently amended) A method ~~for allowing a DMA engine to provide access to a plurality of slave devices to multiple masters, the protocol, implemented by hardware and software on the DMA engine, the master, and the slave devices,~~ comprising ~~the steps of~~:

to implement a direct message transfer to a slave:

accessing a slave status register to read a direct message ready status bit which is set when the slave is ready to transfer data;

transferring message data using a ~~the~~ DMA engine and a slave mailbox register if the direct message ready status bit is set;

setting a ~~an~~ message transfer complete status interrupt at the slave to indicate when the transfer of the message is complete; and

to implement an indirect data transfer to the memory space of a slave device:

accessing a slave status register to read an indirect message ready status bit which is set when the slave is ready to transfer data;

transferring address data using the DMA engine and slave indirect address mailbox register if the indirect message ready status bit is set;

setting an indirect transfer message interrupt bit at the slave to initiate the indirect transfer;

transferring message data between the DMA engine and slave mailbox registers if the indirect message ready status bit is set, where the slave utilizes its own memory map and the address data to transfer data between a location indicated by the address data and the DMA engine; and

setting a ~~an~~ message transfer complete status interrupt at the slave to indicate when the transfer of the message is complete.

6. (currently amended) The method of claim 5 further comprising ~~the step of~~:

negotiating with all the slaves to implement either an asynchronous, synchronous, or source synchronous data transfer.

7. (currently amended) The method of claim 5 further comprising ~~the step of~~:

starting the bus upon reset at a fixed bus-width and then negotiating with all the slaves to implement acceptable bus bit-width.

8. (currently amended) A system ~~allowing a DMA engine to provide access to a plurality of slave devices to multiple masters, the protocol, implemented by hardware and software on the DMA engine, the master, and the slave devices, said system~~ comprising:

means for implementing a direct message transfer to a slave device including:

means for accessing a slave status register to read a direct message ready status bit which is set when the slave is ready to transfer data;

means for transferring message data using a ~~the~~ DMA engine and a slave mailbox register if the direct message ready status bit is set;

means for setting a ~~an~~ message transfer complete status interrupt at the slave to indicate when the transfer of the message is complete; and

means for implementing ~~implement~~ an indirect data transfer to the memory space of a slave device including:

means for accessing a slave status register to read an indirect message ready status bit which is set when the slave is ready to transfer data;

means for transferring address data using the DMA engine and slave indirect address mailbox register if the indirect message ready status bit is set;

means for setting an indirect transfer message interrupt bit at the slave to initiate the indirect transfer;

means for transferring message data between the DMA engine and slave mailbox registers if the indirect message ready status bit is set, where the slave utilizes its own memory map and the address data to transfer data between a location indicated by the address data and the DMA engine; and

means for setting a ~~an~~ message transfer complete status interrupt at the slave to indicate when the transfer of the message is complete.

9. (Original) The system of claim 8 further comprising:

means for negotiating with all the slaves to implement either an asynchronous, synchronous, or source synchronous data transfer.

10. (Original) The system of claim 8 further comprising:

means for starting the bus upon reset at a fixed bus-width and then negotiating with all the slaves to implement acceptable bus bit-width.

11. (currently amended) An apparatus ~~A slave device for allowing a DMA engine to provide access by multiple masters, said slave device~~ comprising:

a slave status register accessible ~~accessed~~ to read a direct message ready status bit which is set when the slave is ready to transfer data directly and accessible ~~accessed~~ to read an indirect message ready bit which is set when the slave is ready to transfer data indirectly;

a slave mailbox register configured to transfer ~~for transferring~~ direct message data using a ~~the~~ DMA engine if the direct message ready status bit is set and with the slave mailbox registers used for transferring message data using the DMA engine if an indirect message ready status bit is set;

a message transfer complete status interrupt at the slave configured ~~that is set~~ to indicate when the transfer of the message is complete;

a slave indirect address mailbox register configured to transfer ~~for transferring~~ address data using the DMA engine if the indirect message ready status bit is set;

an indirect transfer message interrupt bit at the slave configured to ~~which is set to~~ initiate the indirect transfer; and

a slave memory map configured for use ~~used~~ with the address data to transfer data between a location indicated by the address data and the DMA engine.